6 September 1993

Commissioner of Patents & Trademarks
Box 9
Washington, D.C. 20231

Dear Sir,

Please send me copies of the following patents:

5,204,556	1993	Programmable interconnect structure for logic blocks
5,191,243	1993	Output logic macrocell with enhanced functional capabilities
5,162,679	1992	Sense amplifier with depletion transistor feedback
5,138,198	1992	Integrated programmable logic device with control circuit to power down unused sense amplifiers
5,130,574	1992	Programmable logic device providing product term sharing and steering to the outputs of the programmable logic device
4,896,296	1990	PROGRAMMABLE LOGIC DEVICE CONFIGURABLE INPUT/OUTPUT CELL
4,887,239	1989	ONE-TIME PROGRAMMABLE DATA SECURITY SYSTEM FOR PROGRAMMABLE LOGIC DEVICE
4,855,954	1989	IN-SYSTEM PROGRAMMABLE LOGIC DEVICE WITH FOUR DEDICATED TERMINALS
4,852,044	1989	PROGRAMMABLE DATA SECURITY CIRCUIT FOR PROGRAMMABLE LOGIC DEVICE
4,766,569	1988	PROGRAMMABLE LOGIC ARRAY
4,761,768	1988	PROGRAMMABLE LOGIC DEVICE
5,086,396	1992	Apparatus and Method For an Aircraft Navigation System
5,001,647	1991	Inertial Transformation Matrix Generator
5,072,396	1991	Digital Map Correlation
5,223,844	1993	Vehicle tracking and security system

5,216,611	1993	Integrated enroute and approach guidance system for aircraft
5,214,757	1993	Interactive automated mapping system
5,210,540	1993	Global positioning system
5,179,519	1993	Navigation system for vehicle
5,153,836	1992	Universal dynamic navigation, surveillance, emergency location, and collision avoidance system and method
5,148,524	1992	Dynamic video RAM incorporating on chip vector/image mode line modification
5,148,523	1992	Dynamic video RAM incorporationg on chip line modification
5,142,637	1992	Dynamic video RAM incorporating single clock random port control
5,210,639	1993	Dual-port memory with inhibited random access during transfer cycles with serial access
5,206,833	1993	Pipelined dual port RAM
5,201,037	1993	Multi-port memory as a frame buffer
5,198,804	1993	Video memory with write mask from vector or direct input
5,196,834	1993	Dynamic palette loading opcode system for pixel based display
5,195,056	1993	Read/write memory having an on-chip input data register, having pointer circuits between a serial data register and input/output buffer circuits
5,179,372	1993	Video Random Access Memory serial port access
5,170,157	1992	Memory device for an image display apparatus having a serial port and independently operable data registers
5,163,024	1992	Video display system using memory with parallel and serial access employing serial shift registers selected by column address
5,157,776	1992	High speed memory for microcomputer systems
5,157,775	1992	Dual port dual speed image memory access arrangement
5,148,524	1992	Dynamic video RAM incorporating on chip vector/image mode line modification

5,148,523	1992	Dynamic video RAM incorporationg on chip line modification
5,142,637	1992	Dynamic video RAM incorporating single clock random port control
5,121,360	1992	Video random access memory serial port access
5,119,477	1992	Memory manager for hierarchical graphic structures
5,065,368	1991	VIDEO RAM DOUBLE BUFFER SELECT CONTROL
5,042,014	1991	DUAL MEMORY HAVING PIPELINED SERIAL OUTPUT
5,042,013	1991	SEMICONDUCTOR MEMORY
5,042,012	1991	SERIAL ACCESS DYNAMIC RAM
5,023,838	1991	RANDOM ACCESS MEMORY DEVICE WITH INTEGRAL LOGIC CAPABILITY
5,001,672	1991	VIDEO RAM WITH EXTERNAL SELECT OF ACTIVE SERIAL ACCESS REGISTER
4,987,559	1991	SEMICONDUCTOR MEMORY DEVICE HAVING A PLURALITY OF ACCESS PORTS
4,984,214	1991	MULTIPLEXED SERIAL REGISTER ARCHITECTURE FOR VRAM
4,897,818	1990	DUAL-PORT MEMORY WITH INHIBITED RANDOM ACCESS DURING TRANSFER CYCLES
4,893,280	1990	DUAL PORT RANDOM ACCESS MEMORY HAVING VARIABLY CUSTOMIZED ORGANIZATION OF MEMORY BIT UNITS
4,891,794	1990	THREE PORT RANDOM ACCESS MEMORY
4,870,621	1989	DUAL PORT MEMORY DEVICE WITH IMPROVED SERIAL ACCESS SCHEME
4,866,678	1989	DUAL MEMORY HAVING PIPELINED SERIAL OUTPUT
4,858,190	1989	DUAL PORT SEMICONDUCTOR MEMORY HAVING RANDOM AND SERIAL ACCESS MODES
4,833,649	1989	MULTIPLE PORT RANDOM ACCESS MEMORY
4,825,411	1989	DUAL MEMORY WITH ASYNCHRONOUS CONTROL OF SERIAL DATA MEMORY TRANSFER
4,821,226	1989	DUAL PORT VIDEO MEMORY SYSTEM HAVING A BIT-SERIAL ADDRESS INPUT PORT

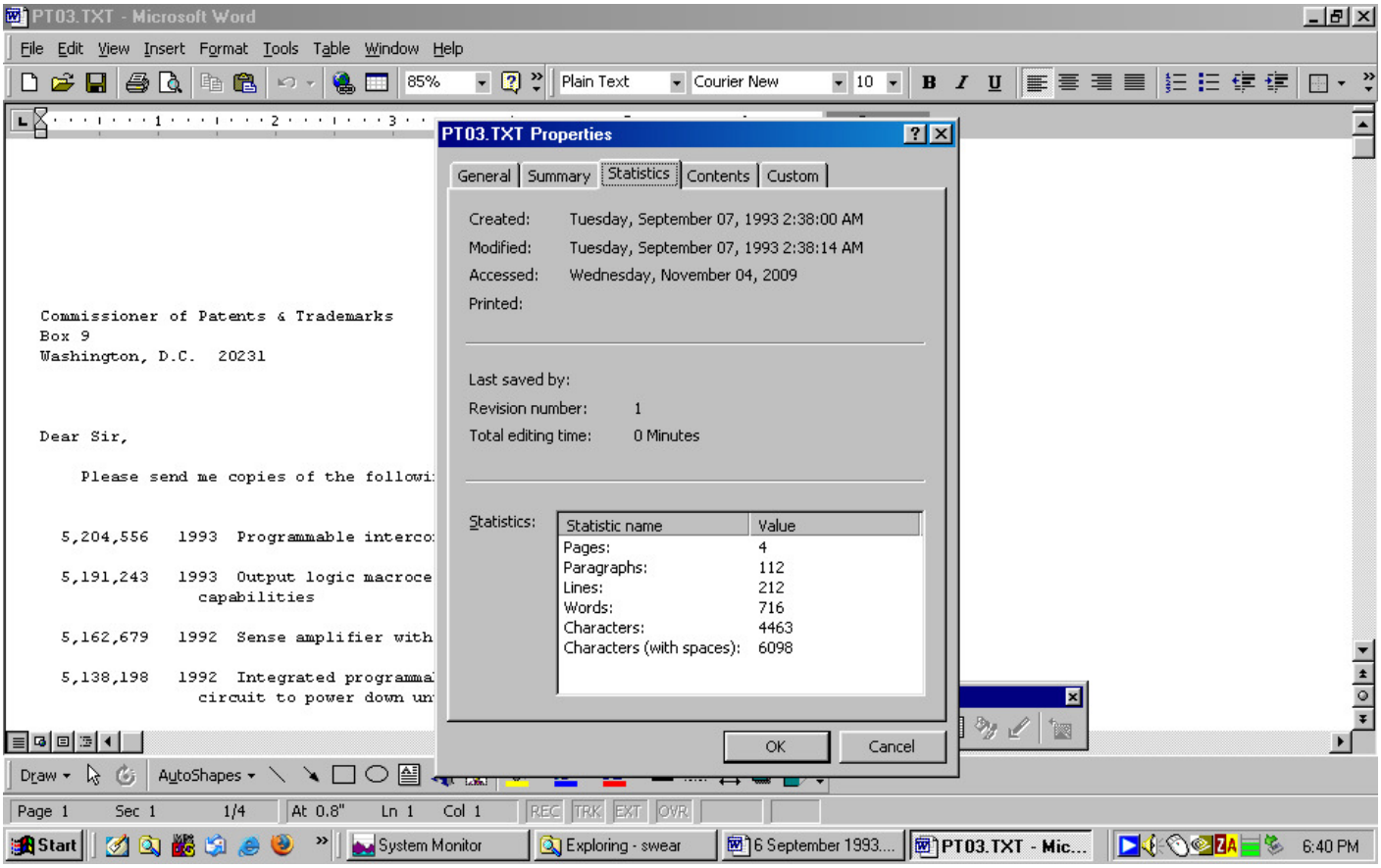
4,817,051	1989	EXPANDABLE MULTI-PORT RANDOM ACCESS MEMORY
4,789,960	1988	DUAL PORT VIDEO MEMORY SYSTEM HAVING SEMI-SYNCHRONOUS DATA INPUT AND DATA
4,747,081	1988	VIDEO DISPLAY SYSTEM USING MEMORY WITH PARALLEL AND SERIAL ACCESS EMPLOYING SERIAL SHIFT REGISTERS SELECTED BY COLUMN ADDRESS
4,719,601	1988	COLUMN REDUNDANCY FOR TWO PORT RANDOM ACCESS MEMORY
4,689,741	1987	VIDEO SYSTEM HAVING A DUAL-PORT MEMORY WITH INHIBITED RANDOM ACCESS DURING TRANSFER CYCLES
4,663,735	1987	RANDOM/SERIAL ACCESS MODE SELECTION CIRCUIT FOR A VIDEO MEMORY SYSTEM
4,648,077	1987	VIDEO SERIAL ACCESSED MEMORY WITH MIDLINE LOAD
4,644,502	1987	SEMICONDUCTOR MEMORY DEVICE TYPICALLY USED AS A VIDEO RAM
4,639,890	1987	VIDEO DISPLAY SYSTEM USING MEMORY WITH PARALLEL AND SERIAL ACCESS EMPLOYING SELECTABLE CASCADED SERIAL SHIFT REGISTERS

Enclosed is a check for 65 * $3.00 = $195.00 .

Thank you.

Sincerely yours,

Jed Margolin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Dear Sir,
Please send me copies of the followi
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5,191,243 1993 Output logic macroce
capabilities
5,162,679 1992 Sense amplifier with
5,138,198 1992 Integrated programma
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Modified: Tuesday, September 07, 1993 2:38:14 AM
Accessed: Wednesday, November 04, 2009
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JED MARGOLIN
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