IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Jed Margolin

Serial No.: 11/130,939 Examiner: Phung M. Chung

Filed: 05/17/2005 Art Unit: 2117

For: MEMORY WITH INTEGRATED PROGRAMMABLE CONTROLLER

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENTS AND RESPONSE

Dear Sir:

In the Office Action mailed December 28, 2007, Claims 1-3, 5-6, 8, and 10-11 were allowed and Claims 14-16 were rejected. Please enter the following amendments and consider the following remarks.

Amendments to the claims begin on page 2 of this response. Remarks begin on page 7 of this response.

Claim Amendments

Please cancel claims 14-16 without prejudice.

Claim 1. (previously presented) A single chip memory comprising:

(a) a memory array;

(b) a processor;

(c) a processor RAM memory;

(d) a multiplexor;

whereas:

(a) said processor is connected to said processor RAM memory and said multiplexor;

(b) said memory array is also connected to said multiplexor;

(c) said memory array is a read/write memory;

whereby:

(a) said multiplexor controls and arbitrates access between said memory array, said processor, said processor RAM memory, and a user's system;

(b) said user's system uses said multiplexor to store a program into said processor RAM memory;

(c) said processor uses said program in said processor RAM memory to test said memory array; and

whereas said program is an algorithmic test program.

Claim 2. (previously presented) The single chip memory of claim 1 further comprising a non-volatile memory connected to said processor, said processor RAM memory, and said mulitiplexor.

Claim 3. (previously presented) The single chip memory of claim 1 further comprising a programmable clock connected to said processor.

Claim 4. (canceled)

Claim 5. (previously presented) The single chip memory of claim 1 whereby said program is also used by said processor to perform one or more functions selected from a group comprising data pattern matching, moving data, graphics primitives, data encryption, and data decryption.

Claim 6. (previously presented) A single chip memory comprising:

(a) a memory array;

(b) a processor;

(c) a processor RAM memory;

(d) a multiplexor;

(e) a non-volatile memory;

whereas:

(a) said processor is connected to said processor RAM memory, said multiplexor, and said non-volatile memory;

(b) said memory array is also connected to said multiplexor;

(c) said memory array is a read/write memory;

whereby:

(a) said multiplexor controls and arbitrates access between said memory array, said processor, said processor RAM memory, said non-volatile memory, and a user's system;

(b) said user's system uses said multiplexor to store a program into said processor RAM memory;

(c) said processor uses said program in said processor RAM memory to test said memory array;

(d) said processor uses said non-volatile memory to store the results of said program in said processor RAM memory used to test said memory array; and

whereas said program is an algorithmic test program.

Claim 7. (canceled)

Claim 8. (previously presented) The single chip memory of claim 6 further comprising a programmable clock connected to said processor.

Claim 9. (canceled)

Claim 10. (previously presented) The single chip memory of claim 6 whereby said program is also used by said processor to perform one or more functions selected from a group comprising data pattern matching, moving data, graphics primitives, data encryption, and data decryption.

Claim 11. (previously presented) A single chip memory comprising:

(a) a memory array;

(b) a processor;

(c) a processor RAM memory;

(d) a multiplexor;

(e) a non-volatile memory;

(f) a programmable clock;

whereas:

(a) said processor is connected to said processor RAM memory, said multiplexor, and said non-volatile memory;

(b) said memory array is also connected to said multiplexor;

(c) said memory array is a read/write memory;

(d) said programmable clock is connected to said processor;

whereby:

(a) said multiplexor controls and arbitrates access between said memory array, said processor, said processor RAM memory, said non-volatile memory, and a user's system;

(b) said user's system uses said multiplexor to store a program into said processor RAM memory;

(c) said processor uses said program in said processor RAM memory to test said memory array;

(d) said processor uses said non-volatile memory to store the results of said program in said processor RAM memory used to test said memory array; and

whereas said program is an algorithmic test program.

Claim12. (canceled)

Claim13. (canceled)

Claim 14. (canceled)

Claim 15. (canceled)

Claim 16. (canceled)

REMARKS

In the Office Action mailed December 28, 2007, Claims 1-3, 5-6, 8, and 10-11 were allowed and Claims 14-16 were rejected.

Applicant has canceled Claims 14-16 and therefore submits that the application as amended is in condition for allowance.

Respectfully submitted,

/Jed Margolin/ Date: January 24, 2008
Jed Margolin

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